REMARKS

Claim 16 is amended herein. Claims 1-24 are pending. The specification is amended herein to correct minor informality and inadvertent errors. No new matter has been introduced. Support for amendment to claim 16 can be found in the Specification, particularly on page 18, lines 1-17. Applicant respectfully submits that these amendments do not change the scope or the subject matter of the claimed invention. Applicant further submits that, by the amendments presented herein, the present application is in a condition for allowance.

Independent claims 1 and 2 and their respective dependent claims 3, 6-8, 10, 12-13, 16-17, and 23-24 were rejected under 35 U.S.C. § 102(e) as being anticipated by Howe et al. (U.S. Pat. No. 6,210,988, hereinafter "Howe"). Dependent claims 4-5, 9, 11, 14-16, and 18-22 were not rejected on the merits but were considered as containing "non-limitation". Dependent claims 7-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Howe in view of Yao (U.S. Pat. No. 5,578,976). Dependent claims 23-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Howe in view of Mitchell (U.S. Pat. No. 5,573,679). The rejections are respectfully traversed herein and reconsideration is hereby earnestly solicited.

Regarding 35 U.S.C. § 112, second paragraph, rejection

Claim 16 was rejected under this paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as his invention. In particular, the examiner contended that the phrase "wherein said correlated curvature essentially reduces with the square of an increase of the variable sputtered layer thickness for constant remaining first sputtering criteria" was not clear. Claim 16 is amended herein to more particularly point out and distinctly claim that the correlated curvature essentially decreases with an increase of the variable sputtered layer thickness. The claim language of claim 16, original and amended, can be found on page 18, lines 1-17, of the specification. No new matter is introduced. It is submitted that claim 16 as amended overcomes the indefiniteness rejection.

Overview of the invention

A primary object of the present invention is to provide a micro-machined structure [Spec., page 5, lines 15-18] that can be fabricated non-destructively to and in combination with a pre-fabricated aluminum-metalized electronic circuitry, i.e., an operational circuitry, such as an aluminum-metalized CMOS circuitry [Spec., page 8, lines 17-26]. This goal is achieved in a microstructure made of sputtered silicon [Spec., page 1, line 28, page 6, lines 9-16].

As specifically discussed in the detailed description of the specification with reference to the drawings, the sputtered silicon structured is positioned on a work piece and being formed on top of a sacrificial layer. The work piece may be a substrate, e.g., **1** in Fig. 1, or any structure including a substrate known to those skilled in the art as a base for micro-machined structures and electronic circuitry [Spec., page 11, lines 31-32, page 12, lines 1-11]. The work piece according to the present invention is a unit undividedly exposed to the fabrication steps required for fabricating micro-machined structures including a thermal annealing process [*id.*]. The work piece may include pre-fabricated electronic circuitry having a critical thermal budget which the circuitry configuration becomes permanently altered [*id.*].

The fabrication of the sputtered silicon structure is accomplished with a thermal fabrication budget [Spec., page 25, lines 16-19] that is lower than the critical thermal budget of the pre-fabricated electronic circuitry of the work piece and/or the critical thermal budget of the sacrificial layer, e.g., **2** in Fig. 1. This low thermal fabrication budget is crucial to the inventive sputtered silicon structure in that it allows for direct non-destructive integration of micro-machined structures to pre-fabricated operational circuitry.

The thermal fabrication budget according to the present invention includes a thermal sputtering budget and a thermal annealing budget for the optional low temperature annealing process [*id.*]. The sputtering process, with deposition temperature approximately between room temperature and 200°C, is particularly discussed in the specification on page 12, lines 13-32, and on page 13, lines 1-9, with reference to Fig. 1. The annealing process, with a maximum annealing temperature of 350°C, is particular discussed in the specification on page 13, lines 11-29, with reference to Fig. 2.

As distinguished on page 2, lines 3-15, of the specification, prior art LPCVD process requires much higher deposition temperature of 580-630°C and annealing temperature of above 900°C. Since electronic circuitry is typically heat resistant only up to temperatures below those required for the LPCVD process, this means the metal layers of the electronic circuitry will have to be deposited after the polysilicon deposition or refractory metals such as tungsten instead of aluminum. Both approaches require re-engineering the CMOS process to accommodate the new thermal budget, metal layers, and/or lithography changes.

Sputtered silicon, however, can be used to make released microstructures atop standard, aluminum-metalized CMOS at temperatures below 350°C. By avoiding the temperature extremes of LPCVD polysilicon, the number of foundry CMOS processes available to the MEMS designer increases dramatically, resulting in potentially significant cost-savings and performance advantages. Additionally, because sputtered silicon can be deposited at low temperatures, other sacrificial layers, such as polyimide, are also viable. These organic sacrificial layers have the advantage of releasing in oxygen plasma, eliminating the need for protective layers for the CMOS circuitry. The sputtered layer of the sputtered silicon structure is porous and permeable to HF-based etches at approximately ten times the thickness reported for LPCVD deposited polysilicon [Spec., page 9, lines 14-26].

Regarding 35 U.S.C. § 102(e) rejections

Independent claims 1 and 2 and their respective dependent claims 3, 6-8, 10, 12-13, 16-17, and 23-24 were rejected under this paragraph as being anticipated by Howe. Rejections directed to the dependent claims are collectively traversed hereinafter with respect to independent claims 1 and 2.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

It is respectfully submitted that Howe's patent does not teach or anticipate the invention as claimed. Howe does not teach each and every element as set forth in the claims, either expressly or inherently described, because, among others, **a) "sputtered silicon structure" is nowhere to be found in Howe**, including cited column 3, lines 1-9; **b) Howe's process requires at least 30 percent of germanium**; and **c) Howe explicitly lacks any teachings on sputtering process.**

The poly-silicon-germanium (poly-$Si_{(1-x)}Ge_x$, where $0<x\leq 1$) is a semiconductor alloy material having physical properties similar to polysilicon [col. 4, lines 26-34]. Howe particularly chose germanium (Ge) or germanium-rich poly-SiGe films because Ge has higher absorption coefficient than silicon (Si), resulting in selective heating of Ge [col. 5, lines 54-67]. As such, by increasing the Ge content, the deposition temperature thus can be lowered, achieving a low deposition temperature at 325°C for **pure Ge** [col. 5, lines 16-23].

Specifically, Howe teaches a LPCVD poly-silicon-germanium (poly-$Si_{(1-x)}Ge_x$) process including depositing a sacrificial layer of silicon-germanium onto a substrate, depositing a structural layer of silicon-germanium onto the sacrificial layer, where the germanium content of the sacrificial layer is greater than the germanium content of the structural, and removing at least a portion of the sacrificial layer [col. 1, lines 66-67, through col. 2, lines 1-6]. The deposition temperature is about 650°C. As discussed before, the deposition temperature can be lowered by increasing the Ge content, down to 325°C for 100% Ge [col. 5, lines 16-23]. According to Howe, the minimum Ge content in the sacrificial layer and the structural layer is about 30 percent [col. 5, lines 24-25]. Without Ge, there would be no selective heating and thus no reduced deposition temperature. In other words, the absence of Ge would destroy the function and purpose of Howe's invention.

Contrastingly, as discussed heretofore in the Overview section and in the detailed description of the specification, the claimed invention is a "**sputtered silicon structure**" and **does not require any Ge content** to achieve a low thermal fabrication budget where the deposition temperature is approximately between room temperature and 200°C [Spec., page 12, lines 19-30]. Howe's LPCVD poly-silicon-germanium microstructures are inherently, clearly, and patently distinct from the claimed sputtered silicon structure.

Moreover, Howe **does not teach or anticipate utilizing sputtering deposition to produce a sputtered silicon structure.** In fact, Howe teaches away from the claimed invention in that Howe specifically discloses that "[c]onventional low pressure chemical vapor deposition (LPCVD) equipment can be used to conformally deposit poly-SiGe films [col. 5, lines 9-11] and that an LPCVD Si furnace can be converted to a SiGe furnace simply by adding anther input gas [col. 3, lines 64-65]. As distinguished heretofore in the Overview section and in the detailed description of the specification, LPCVD is fundamentally different and patently distinguishable from the sputtering deposition.

For at least these reasons, Applicant respectfully submits that the claimed sputtered silicon structure is patentably distinct from and not anticipated by Howe's poly-SiGe microstructures. In particular, Applicant respectfully submits that independent claims 1 and 2 respectively recites subject matter not reached by the applicable prior art under 35 USC § 102(e). As such, it is submitted that independent claims 1 and 2 are patentable and therefore should be allowed.

Reliance is placed on *In re* Fine, 5 USPQ 2d 1596, 1600 (Fed. Cir. 1988) and *Ex parte* Kochan, 131 USPQ 204 (Bd. App. 1960) for allowance of the dependent claims 3-24, since they differ in scopes from their parent independent claims 1 and 2 which are submitted as patentable.

Regarding claims 4-5, 9, 11, 14-15, and 18-22

These dependent claims were not rejected on the merits (patentability, *see*, MPEP 706) of the present application under utility provisions of 35 U.S.C. 101, novelty provisions of 35 U.S.C 102 and/or non-obviousness provisions of 35 U.S.C. 103. The examiner's comments and citation of case laws regarding "product by process" claims are confusing, especially in light of the statement that "a rejection based on sections 102 or 103 is fair" (page 4) but none of these claims were rejected based on sections 102 or 103 over any prior art.

Moreover, as stated in MPEP 2173.05(p), "[t]here are many situations where claims are permissively drafted to include a reference to more than one statutory class of invention.

A product-by-process claim, which is a product claim that defines the claimed product in terms of the process by which it is made, is proper (citation omitted.)".

Dependent claims 4-5, 9, 11, 14-15, and 18-22 serve to respectively further define (limit) the claimed product of independent claims 1 and 2 and are submitted to be proper and limiting.

MPEP 2113 states, "even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself." Accordingly, patentability of dependent claims 4-5, 9, 11, 14-15, and 18-22 would be based on the product itself recited in the independent claims 1 and 2. Since claims 1 and 2 are submitted herein as patentable, these dependent claims, which differ only in scopes from their respective parent independent claims 1 and 2, are correspondingly submitted as patentable.

Regarding 35 U.S.C. 103(a) rejections

Dependent claims 7-8 were rejected under this paragraph as being unpatentable over Howe in view of Yao. Dependent claims 23-24 were rejected under this paragraph as being unpatentable over Howe in view of Mitchell. The rejections are respectively traversed for similar reasons. That is, the alleged respective combinations of Howe and Yao and Howe and Mitchell, respectively, do not teach or suggest the claimed "sputtered silicon structure" because the both of the alleged respective combinations **must contain at least 30 percent of Ge as required by Howe.** As is apparent to one skill in the art, poly-SiGe and Si are not equivalents. What is more, the LPCVD process is patently distinguishable from the sputtering process. At best, the alleged combinations would respectively produce CVD-processed poly-SiGe microstructures and thus respectively fail to teach or suggest a "sputtered silicon structure" as claimed.

On the other hand, assuming it were possible for one skilled in the art to modify Howe with Yao or Mitchell, respectively, without Ge, **the lack of Ge content in the respective modifications/combinations would destroy the function and intended purpose of the primary reference Howe**, as previously discussed herein. Thus, there would be no technological motivation for combining and/or modifying Howe with Yao or Mitchell,

respectively. As such, neither Howe and Yao nor Howe and Mitchell are properly combinable and a *prima facie* case of obviousness cannot properly be made regarding the applicant's invention. See *in re* Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

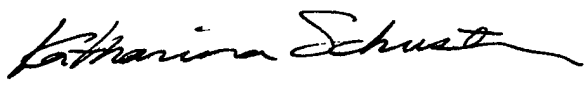
At least for these reasons, it is respectfully submitted that none of the cited references teach or suggest the claimed sputtered silicon structure. "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine,* 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Since obviousness cannot be established absent some teaching, suggestion or incentive supporting the modification/combination, the Examiner has not established a *prima facie* case of obviousness (ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F. 2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984)). Absent such a showing in the prior art, the Examiner has impermissibly used the applicant's teaching to hunt through the prior art for the claimed elements and combine them as claimed (see In re Vaeck, 947 F. 2d 488, 20 USPQ 2d 1438 (Fed. Cir. 1991); In re Bond, 910 F. 2d 831, 15 USPQ 2d 1566 (Fed. Cir. 1990); In re Laskowski, 871 F. 2d 115, 117, 10 USPQ 2d 1397, 1398 (Fed. Cir. 1989)). The use of hindsight is never permissible to establish obviousness." Accordingly, claims 7-8 and 23-24 respectively recite subject matter not reached by the applicable prior art under 35 USC § 103(a) and thus are submitted to be patentable.

This Response is submitted as proper and complete in that it places the application in condition for allowance. Particularly, the present Response is submitted as not adding new matters and not requiring further searches. Since the Examiner has done a thorough search in the first action in light of the disclosure and claims, no new search would be necessary. Accordingly, Applicant respectfully submits that, by the amendments presented herein, the present application is in a condition for allowance.

Since all of the claims pending in the present application are now clearly allowable, favorable consideration and a Notice of Allowance of all the claims are earnestly solicited. The

Examiner is invited to telephone the undersigned at (408) 260-7300 extension 23 for discussing an Examiner's Amendments or other suggested actions for accelerating prosecution and moving the present application to allowance.

Respectfully submitted,



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MARKED-UP VERSION OF THE REPLACEMENT PARAGRAPHS

Please insert the following section after line 10 on page 1:

-- **CROSS-REFERENCE TO RELATED APPLICATIONS**

This application claims the benefit of U.S. provisional patent application No. 60/165,013, filed on November 12, 1999, which is hereby incorporated herein by reference in its entirety.--

On page 3, please replace the second paragraph, lines 9-25, with the following paragraph:

--Stresses and strain gradients can limit the performance of both integrated and passive electrostatic MEMS devices. If the in-plane residual stress in doubly supported structures, for example, is too large, the structures may buckle. Conversely, if the stresses are too large the mechanical stiffness may be too large for the intended application. Stress control in sputtered structures has been achieved previously with high temperature anneals as is described, for example, in T. Abe and M. L. Reed, "Low Strain Sputtered Polysilicon for Micromechanical Structures," Proc[,], of Ninth International Workshop on Micro Electro-Mechanical Systems, San Diego Feb., 1996, pp. 258-262. These high temperature anneals (>1000°C) exceed their thermal annealing budget critical thermal budgets of integrated circuitry. The critical thermal budget is the budget beyond which the configuration of the integrated circuitry becomes permanently changed.--

On page 4, please replace the first paragraph, lines 1-21, with the following:

--forming clusters on top of the sacrificial layer before reaching a closing thickness at which the sputtered silicon

clusters have laterally extended and sufficiently overlapped to form a solid layer. The closing thickness is within several 100 Angstroms. The sputtered silicon within that closing thickness has a specific internal stress that differs significantly from the internal stress of the silicon deposited above the closing thickness. The phenomenon of the differing internal stress within the closing thickness is known to those skilled in the art [closing of the initial clusters<>] as coalescence. The closing thickness is highly constant and introduces an essentially constant coalescence strain to the final structure. With increasing overall thickness of the micro-machined structure the influence of the coalescence strain becomes less influential. Depending upon the application, several additional properties may be important for the structural layer of a micro-fabricated device. Among these characteristics are film density, surface roughness and electrical resistivity, and permeability.--

On page 6, please replace the first paragraph under "SUMMARY", lines 9-16, with the following paragraph:

--A sputtered layer is introduced. The sputtered layer, preferably from silicon, is deposited with predetermined sputtering criteria resulting in a predetermined [resulting<> or] pre-annealing configuration. This pre-annealing configuration is transformed during a low temperature annealing process into a post-annealing configuration. A released structure is micro-machined from the sputtered layer in its post-annealed configuration.--

On page 6, please replace the bottom paragraph, lines 26-32, with the following paragraph:

--The released structure has a resulting [in-plain]in-plane strain and a resulting strain gradient, which are predetermined in accordance with deformation configurations of the released structure. The deformation configuration depends on the shape of the released structure and on the fashion it is supported. The deformation configurations are distinguished between an essentially buckling-free deformation--

On page 8, please replace the second paragraph, lines 5-15, with the following paragraph:

--For buckling-influenced deformation configurations, second sputtering criteria predominantly include and sacrificial layer material are defined such that the sputtered layer has a predetermined resulting or initial [in-plain]in-plane strain. Sputtering power, ambient sputtering pressure and sputtering temperature are selected from a zone-T of the Thornton zone diagram as known to those skilled in the art. In the case, where a low temperature annealing is included in the fabrication process, the second sputtering criteria are selected in correlation with the annealing transformation.--

On page 9, please replace the second paragraph, lines 14-26, with the following paragraph:

--The sputtered layer made from silicon is porous and permeable to HF-based etches at approximately ten times the thicknesses reported for LPCVD deposited polysilicon. The initial porosity remains mostly unaltered during the annealing process such that encapsulated cavities with relatively thick cover layers may be fabricated compared to those made from polysilicon.[.] Consequently, larger and/or more solid cover layers may be

fabricated compared to those from prior art methods. The cover layers are stiffer and better able to withstand the capillary forces of the wet etch in the encapsulated cavity beneath the silicon during a drying process. The annealing need not be performed prior to the release etching.--

On page 12, please replace the bottom paragraph, lines 19-32, with the following paragraph:

--The sputtering process **Sp** is either defined by first sputtering criteria **P1** or by second sputtering criteria **P2**. The first sputtering criteria **P1** provide an initial sputtered layer **3A** having a first pre-annealing configuration including a predetermined initial strain gradient. The second set of sputtering criteria provides the initial sputtered layer 3A having a second pre-annealing configuration including a predetermined initial in-plane strain. The sputtering process should be of zone-T type to ensure that low stresses are achieved. The deposition temperature should thus be approximately between room temperature and 200°C. An Ar working gas deposition pressure ranging from 8 to 14 mTorr yielded acceptable stresses. Films deposited at 8 mTorr were more dense. Those--

On page 13, please replace the bottom paragraph, lines 11-29, with the following paragraph:

--**Fig. 2** shows a simplified section of the work piece of **Fig. 1** during the annealing process. The simplified section of **Fig. 2** features optional aluminum terminals **Al**, which may be deposited after the deposition of the initial sputtered layer **3A** and before the work piece is exposed to a low temperature annealing process **TAn** indicating in **Fig. 2** a rectangle labeled **TB** for a

thermal annealing budget **TB** induced on the work piece during the low temperature annealing process **TAn**. The definition of the thermal annealing budget **TB** includes a maximum annealing temperature and an annealing duration. The thermal annealing budget **TB** is smaller than the critical thermal budget of eventual electronic circuitry of the work piece simultaneously exposed to the low temperature annealing process **TAn**. The films were annealed in nitrogen and a nitrogen-hydrogen environment at temperatures at or below 350°C. The films annealed in the nitrogen-hydrogen environment showed a marked decrease in conductivity and a decrease in the strain gradient.--

MARKED-UP VERSION OF THE AMENDED ABSTRACT

--A sputtered silicon layer and a low temperature fabrication method thereof, is introduced. The sputtered silicon layer[, ,] is sputtered with predetermined sputtering criteria resulting in a predetermined pre-annealing configuration. The sputtering criteria include sputtering power, ambient sputtering pressure, choice of sacrificial layer and etchant. The initially sputtered layer is transformed during a low temperature annealing process into a post-annealing state. A released structure is micro-machined from the sputtered layer in its post-annealed state. The low temperature annealing leaves pre-fabricated integrated aluminum-metalized circuitry unaffected. Optional conductive sputtered co-layers reduce resistivity and may be used to further tune strain and strain gradient.--

MARKED UP VERSION OF THE AMENDED CLAIMS

16) (Amended) The sputtered silicon structure of claim 13 having a variable sputtered layer thickness and a correlated curvature, wherein said correlated curvature essentially [reduces] decreases with [the square of] an increase of the variable sputtered layer thickness [for constant remaining first sputtering criteria].